Page 2 Dkt: 303.871US1

IN THE CLAIMS

1. (Original) A method comprising:

providing a semiconductor substrate that includes a memory container having a double-sided capacitor; and

vapor phase etching a layer adjacent to the side wall of the memory container with a vapor having a surface tension lowering agent.

- 2. (Original) The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having a carboxylic.
- 3. (Original) The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having a carboxylic.
- 4. (Original) The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching an oxide layer adjacent to the side wall of the memory container.
- 5. (Original) The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent comprises vapor phase etching a borophosphosilicate glass (BPSG) material adjacent to the side wall of the memory container.
- 6. (Original) The method of claim 1, wherein vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having the surface tension lowering agent

comprises vapor phase etching the layer adjacent to the side wall of the memory container with the vapor having hydrogen fluoride and an etch initiator composition.

7. (Original) A method comprising:

providing a semiconductor substrate that includes a double-sided capacitor memory container; and

etching a layer adjacent to a side wall of the double-sided capacitor memory container with a vapor that includes methanol.

- 8. (Original) The method of claim 7, wherein etching the layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol comprises etching an insulator layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol.
- 9. (Original) The method of claim 7, wherein etching the layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol comprises etching a doped oxide layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol.
- 10. (Original) The method of claim 7, wherein etching the layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes methanol comprises etching an insulator layer adjacent to the side wall of the double-sided capacitor memory container with the vapor that includes hydrogen fluouride.
- (Original) A method of fabricating a semiconductor substrate, the method comprising: 11. placing a semiconductor substrate that includes a double-sided capacitor container in a chamber; and

Page 4 Dkt: 303.871US1

Serial Number: 10/789,800 Filing Date: February 27, 2004

Title: SEMICONDUCTOR FABRICATION THAT INCLUDES SURFACE TENSION CONTROL

vapor phase etching a layer adjacent to a side wall of the double-sided capacitor container with a vapor that includes hydrogen fluouride, an etch initiator composition and an alcohol.

- 12. (Original) The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching an oxide layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol.
- 13. (Original) The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching an insulator layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol.
- 14. (Original) The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching a layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and a methanol.
- 15. (Original) The method of claim 11, wherein vapor phase etching the layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, the etch initiator composition and alcohol comprises vapor phase etching a layer adjacent to the side wall of the double-sided capacitor container with the vapor that includes hydrogen fluoride, H₂O and an isopropyl alcohol.
- 16. (Original) A method of fabricating an integrated circuit, the method comprising:

Page 6

Dkt: 303.871US1

vapor phase etching of a layer of an insulator material formed adjacent to the side wall, wherein the vapor phase etching comprises:

> mixing a hydrogen fluoride and an isopropyl alcohol to form a mixed vapor; and inserting the mixed vapor into the chamber.

- (Original) The method of claim 21, further comprising heating the hydrogen fluoride and 22. the isopropyl alcohol prior to inserting the mixed vapor into the vapor etch chamber.
- (Original) The method of claim 21, wherein mixing the hydrogen fluoride and the 23. isopropyl alcohol to form the mixed vapor comprises mixing the hydrogen fluoride, the isopropyl alcohol and an etch initiator composition to form the mixed vapor.
- (Original) The method of claim 21, wherein vapor phase etching of the layer of the 24. insulator material formed adjacent to the side wall comprises vapor phase etching of a layer of oxide formed adjacent to the side wall.
- 25. (Original) The method of claim 21, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall comprises vapor phase etching of a layer of silicon dioxide formed adjacent to the side wall.
- 26. (Original) A method for fabricating a semiconductor substrate, the method comprising: placing the semiconductor substrate that includes a memory container into a vapor etching chamber, wherein a side wall of the memory container includes a double-sided capacitor; and

vapor phase etching of a layer of an insulator material formed adjacent to the side wall of the memory container, wherein the vapor phase etching comprises:

mixing an etch initiator composition, hydrogen fluoride and alcohol to form a mixed vapor;

Page 7

Dkt: 303.871US1

heating the mixed vapor; and

inserting the mixed vapor into the vapor etching chamber.

27. (Original) The method of claim 26, wherein mixing the etch initiator composition, hydrogen fluoride and alcohol to form the mixed vapor comprises mixing the etch initiator composition, hydrogen fluoride and isopropyl alcohol to form the mixed vapor.

- 28. (Original) The method of claim 26, wherein mixing the etch initiator composition, hydrogen fluoride and alcohol to form the mixed vapor comprises mixing the etch initiator composition, hydrogen fluoride and methanol to form the mixed vapor.
- 29. (Original) The method of claim 26, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall of the memory container comprises vapor phase etching of a layer of silicon nitride formed adjacent to the side wall of the memory container.
- 30. (Original) The method of claim 26, wherein vapor phase etching of the layer of the insulator material formed adjacent to the side wall of the memory container comprises vapor phase etching of a layer of silicon oxynitride formed adjacent to the side wall of the memory container.
- 31. (Original) A method comprising:

placing a semiconductor substrate into a chamber; and

vapor phase etching of an insulator material formed adjacent to a double-sided container on a semiconductor substrate, wherein the vapor phase etching comprises:

forming a vapor that includes an H₂O vapor, an HF gas and a surface tension lowering agent; and

inserting the vapor into the chamber.

Page 8 Dkt: 303.871US1

Serial Number: 10/789,800 Filing Date: February 27, 2004

Title: SEMICONDUCTOR FABRICATION THAT INCLUDES SURFACE TENSION CONTROL

- 32. (Original) The method of claim 31, wherein forming the vapor that includes H₂O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H₂O, hydrogen fluoride and carboxylic.
- 33. (Original) The method of claim 31, wherein forming the vapor that includes H₂O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H₂O, hydrogen fluoride and alcohol.
- 34. (Original) The method of claim 31, wherein forming the vapor that includes H₂O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H₂O, hydrogen fluoride and isopropyl alcohol.
- 35. (Original) The method of claim 31, wherein forming the vapor that includes H₂O, hydrogen fluoride and the surface tension lowering agent comprises forming the vapor that includes H₂O, hydrogen fluoride and methanol.
- 36. (Original) The method of claim 31, wherein vapor phase etching of the insulator material formed adjacent to the double-sided container on the semiconductor substrate comprises vapor phase etching of a silicon dioxide material formed adjacent to the double-sided container on the semiconductor substrate.
- 37. (Original) The method of claim 31, wherein vapor phase etching of the insulator material formed adjacent to the double-sided container on the semiconductor substrate comprises vapor phase etching of a doped oxide material formed adjacent to the double-sided container on the semiconductor substrate.
- 38. (Original) A method for fabricating a memory array, the method comprising:

Dkt: 303.871US1

forming at least one memory container in a borophosphosilicate glass (BPSG) material on a substrate, wherein a side wall of the at least one memory container includes a double-sided capacitor; and

removing at least a part of the BPSG material based on a vapor wet etch operation with a vapor comprised of hydrogen fluoride and alcohol.

- (Original) The method of claim 38, wherein removing the at least a part of the BPSG 39. material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and alcohol comprises removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and isopropyl alcohol.
- 40. (Original) The method of claim 38, wherein removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and alcohol comprises removing the at least a part of the BPSG material based on the vapor wet etch operation with the vapor comprised of hydrogen fluoride and methanol.

41. (Original) A method comprising:

forming at least one memory container in an oxide, wherein a side wall of the at least one memory container includes a double-sided capacitor; and

vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, an etch initiator composition and a surface tension lowering agent.

- (Original) The method of claim 41, wherein forming the at least one memory container in 42. the oxide comprises forming the at least one memory container in silicon oxide.
- 43. (Original) The method of claim 41, wherein vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and a surface tension

Page 10 Dkt: 303.871US1

Serial Number: 10/789,800

Filing Date: February 27, 2004

Title: SEMICONDUCTOR FABRICATION THAT INCLUDES SURFACE TENSION CONTROL

lowering agent comprises vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and an alcohol.

- (Original) The method of claim 41, wherein vapor wet etching of a layer of the oxide 44. with a vapor comprised of hydrogen fluoride, the etch initiator composition and a surface tension lowering agent comprises vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and an isopropyl alcohol.
- (Original) The method of claim 41, wherein vapor wet etching of a layer of the oxide 45. with a vapor comprised of hydrogen fluoride, the etch initiator composition and a surface tension lowering agent comprises vapor wet etching of a layer of the oxide with a vapor comprised of hydrogen fluoride, the etch initiator composition and methanol.

46-95. (Canceled)